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(54) Method of manufacturing a semi-conductor device.

(57) A semi-conductor device is manufactured by forming on a silicon substrate 101, source and drain diffusion layers 103 and 104, an insulation film 102, a gate film 105, a gate electrode 106 and an insulation film 107. A contact hole 108 is formed through the films 107 and 105 and a bottom electrode 109 for a ferro-electric film is formed on the film 107 and in the hole 108. A ferro-electric film 110 of $PbTiO_3$ or PZT or PLZT is sputtered onto the electrode 109 and film 107 and it is treated by ion implantation of Pb to correct the composition thereof to stoichiometric composition. Thereafter, annealing takes place at above 500°C to improve the crystalline characteristics of the film. A top electrode 111 is formed on the shaped film 110 and the whole protected by a passivation layer 112.

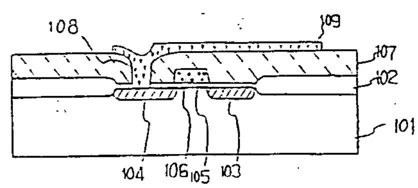

FIG 1 (a)

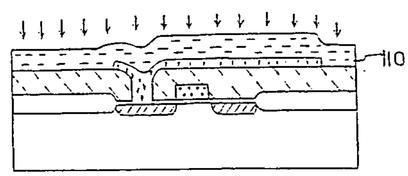

FIG 1 (b)

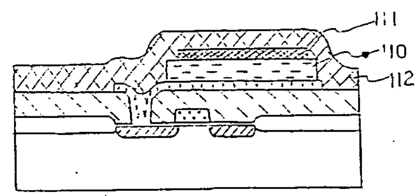

FIG 1 (C)

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EUROPEAN SEARCH REPORT

Application Number

EP 90 30 0752

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X A	JAPANESE JOURNAL OF APPLIED PHYSICS. vol. 17, no. 3, March 1978, TOKYO JP pages 573 - 574; SHINTANI ET AL.: 'Pb(Zr.Ti)O3 films by RF sputtering in PbO vapour' * the whole document * *	1,7,9,12 3-5	C 23 C 14/08 C 23 C 14/06 H 01 L 29/95 H 01 L 21/3205 H 01 L 21/3105 H 01 G 7/06
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 169 (C-587)21 April 1989 & JP-A-63 317 670 (FUJI ELECTRIC CO LTD) 26 December 1988 * abstract * *	1,7,8,12	
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 275 (C-516)29 July 1988 & JP-A-63 053 264 (SUMITOMO ELECTRIC IND LTD) 7 March 1988 * abstract * *	1,2,12	
A	JAPANESE JOURNAL OF APPLIED PHYSICS. vol. 18, no. 8, August 1977, TOKYO JP pages 1633 - 1634; OKUYAMA ET AL.: 'Preparation of PbTiO3 ferroelectric thin film by RF sputtering' * the whole document * *	1,3-5,12	**TECHNICAL FIELDS SEARCHED (Int. Cl.5)**
A	JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY vol. 17, no. 2, March 1980, NEW YORK US pages 629 - 633; CASTELLANO: 'Ion beam deposition of ferroelectric thin films sputtered from multicomponent targets' * page 629, right column * * * page 631, paragraph 1 * *	1,3,4,7,12	C 23 C H 01 L H 01 G C 30 B
A	US-A-4 437 139 (HOWARD) * column 3, line 48 - column 4, line 20 * *	1,3,5,7,12	

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	13 January 92	MES L.A.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document

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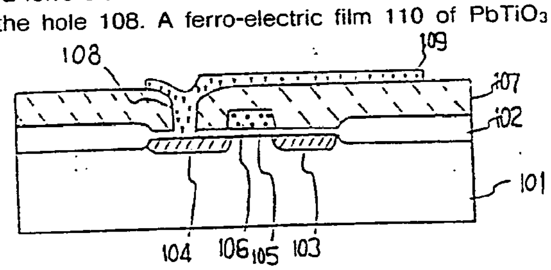

FIG 1 (a)

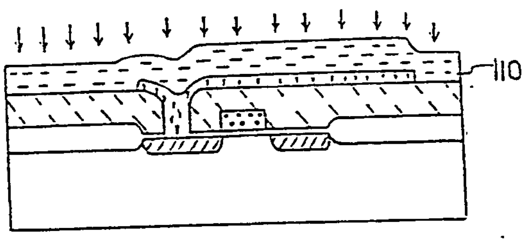

FIG 1 (b)

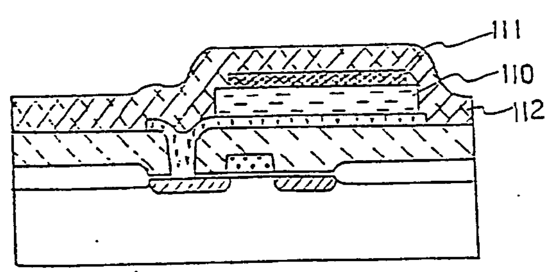

FIG 1 (C)

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METHOD OF MANUFACTURING A SEMI-CONDUCTOR DEVICE

This invention relates to methods of manufacturing semi-conductor devices, in particular, those including a ferro-electric thin film, for example for use in memory devices.

In the prior art, MIS type transistors, which employ the change of surface potential on a silicon substrate caused by introducing electric charge from the substrate to a trap or floating gate within an isolation gate, are used as non-volatile memory. In practice, such non-volatile memory may be used in Erasable and Programmable Read Only Memory (EPROM) and Electrically Erasable Programmable Read Only Memory (EEPROM).

Such non-volatile memory has problems, in that the read/write voltage is usually high, about 20 V, read/write takes a relatively long time, several tens of milli-seconds in the case of EEPROM, and read/write capability is low, being in the order of 10^5 repetitions.

Because the read/write time is theoretically the same in non-volatile memory employing a ferro-electric material which is electrically capable of polarity turn-about, and polarisation is kept, even when the source of electricity is shut off, non-volatile memory employing a ferro-electric film has the potential of being an ideal non-volatile memory. Non-volatile memory employing ferro-electric material has been suggested in, for example, US-A-4,149,302 as an integrated construction of ferro-electric capacitors on a silicon substrate, and US-A-3,832,700 as a non-volatile memory having ferro-electric films laid at the gate of MIS type transistor. In practice, however, non-volatile memory employing a ferro electric material is not of use because ferro-electric thin films are not stable enough and ferro-electric films of stoichimetric composition are hard to be realised. In the case when, for example, PZT ($PbTiO_3/PbZrO_3$) is to be employed as a ferro-electric film, and, for example, sputtering is used for its construction, then the result is an oxide of three elements, and the ratio of Pb, Ti and Zr in the sputtered film does not match the stoichiometric composition. A common method of trying to cope with this problem, is to add more PbO to the sputtering target, but, even in this case, the ratio goes off the stoichiometric composition. Oxygen may be used as a sputtering gas, but a lack of oxygen in the sputtered film occurs. This invention is aimed at a solution to such problems, and its object is to provide a method of manufacturing ferro-electric films with excellent stability and of excellent stoichiometric composition.

According to the invention, therefore, a method of manufacturing a semi-conductor device, comprises the steps of forming a ferro-electric film in the device, and treating the film to improve the stoichiometric composition thereof.

From one aspect of the invention, this is achieved by doping the film by ion implantation after formation of the film.

In this case, to improve the crystalline characteristics thereof, the film may thereafter be annealed, preferably at above 500°C or by rapid thermal anneal.

Annealing may be performed in an atmosphere containing ozone.

From another aspect of the invention, the film is formed by sputtering in an atmosphere containing ozone.

Alternatively, the sputtering may be in an atmosphere containing lead or a lead compound, for example, $PbCl_4$, $Pb(C_2H_5)_4$ and $Pb_2O(OH)_2$.

The preferred main component of the ferro-electric film is at least on of $PbTiO_3$, PZT-($PbTiO_3/PbZrO_3$) and PLZT($La/PbTiO_3/PbZrO_3$).

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figures 1 (a), 1(b) and 1(c) are diagrammatic cross sectional views of a semi-conductor device at successive stages of its manufacture by a method according to this invention;

Figure 2 is a diagrammatic cross sectional view of a sputtering apparatus which may be used in the manufacturing method according to this invention; and

Figure 3 is a similar diagrammatic cross sectional view of another sputtering apparatus which may be used in the method according to the present invention. The manufacturing process according to the invention, will now be described by way of example, as applied to a semi-conductor device including a silicon substrate and an n type channel transistor.

A p type silicon substrate 101 (Figure 1 (a)) with a resistivity of 20 ohm-cm, has n type diffusion layers 103 and 104 formed therein to constitute source and drain of an MOS transistor, by doping $4e^{15} cm^{-2}$ phosphorous by ion implantation. An insulation film 102, approximately 600 nm (6000 Angstroms) thick is deposited by the LOCOS method to isolate the elements. A gate film 105, approximately 30 nm (300 Angstroms) thick is formed as shown. A gate electrode 106 of polysilicon 400 nm (4000 Angstroms) thick is formed on the gate film 105 between the source and drain layers 103 and 104. An inter-layer insulation film 107 is formed by vapour deposition thereon of SiO_2 to a thickness of 600 nm (6000 Angstroms) and a contact hole 108 is formed through the films 107 and 105 to expose the diffusion layer 104. Thus far, the steps of the

manufacturing process are known from the prior art and may be varied in accordance with the particular form of semi-conductor device required.

Next, a bottom electrode 109 for a ferro-electric film is formed upon the film 107 and through the contact hole 108. The film 109 may be of aluminium, deposited by sputtering to a thickness of 1000 nm. Using known photo-lithography methods, the film is formed to a prescribed pattern. This may be done after formation of the ferro-electric film or even after formation of a top electrode upon the ferro-electric film, as described hereinafter. In some cases, to affect the crystalline characteristics of the subsequently deposited ferro-electric film, the film 109 may be of platinum.

Then, a ferro-electric film 110 (Figure 1 (b)) of $PbTiO_3$ is formed over the film 109 by sputtering to a thickness of, for example, 500 nm (5000 Angstroms). The target for the sputtering is of stoichiometric composition. Then the ferro-electric film 110 is doped by ion implantation at 100 kV, and $5e^{15}cm^{-2}$ of Pb is implanted. The film 110 is then annealed, for example in a nitrogen atmosphere at approximately 550° C for one hour.

The ferro-electric film 110 (Figure 1 (c)) is then formed to a prescribed shape using photo-lithography, and a top electrode 111 is formed thereon, for example, by sputtering aluminium to a thickness of 500 nm (5000 Angstroms). The top electrode 111 is then shaped and a passivation layer 112 is formed over the whole device, for example by plasma CVD deposition of a SiN film.

The target is of stoichiometric composition, but deviations from stoichiometric composition occur in the sputtered film. These, according to one aspect of the invention, can be corrected by ion implantation to produce a ferro-electric film of stoichiometric composition. If the ferro-electric film becomes amorphous by such ion implantation, then annealing produces a ferro-electric film with excellent crystalline characteristics. This improves the data retention capability of such devices over that of devices in the prior art, for example from eight months to one and a half years. Also, the read/write capability is improved approximately one hundredfold, from 10^5 to 10^7.

Whilst $PbTiO_3$ is the principal component of the ferro-electric film described, it will be understood that other materials may be used and similar improvements achieved. In particular, PZT-($PbTiO_3$/$PbZrO_3$) or PLZT(La/$PbTiO_3$/$PbZrO_3$) may be used and remarkable results obtained.

Sputtering of the ferro-electric film may take place in sputtering apparatus such as is shown diagrammatically in Figure 2. A silicon wafer 202 is placed upon an upper electrode 201, and a sintered target 204 is placed upon a bottom electrode 203. The target 204 is, for example, of PZT (65% $PbZrO_3$ and 35% $PbTiO_3$). A radio frequency source 205 of electricity is connected across the electrodes 201 and 203 and operates during sputtering. Sputtering gases are introduced through passages 206, 207 and 208. Usually, the gases are argon, oxygen and ozone, though the latter need not always be used. The ratio of such gases may, with advantage, by 80% Ar; 15% O_2; 5% O_3. With the use of ozone, lack of oxygen in the sputtered film does not occur, as the reaction of ozone is very high. This avoids the need for subsequent ion implantation with oxygen. A similar result may be achieved by subsequent annealing in an atmosphere containing ozone after sputtering in an atmosphere of argon and oxygen. Improvement of the crystalline structure of the ferro-electric film is obtained by annealing at above 500° C. Good crystalline characteristics may be achieved by a rapid thermal anneal.

Another sputtering apparatus for use in the invention is shown diagrammatically in Figure 3. In this, a silicon wafer 302 is placed upon a top electrode 301, and a sintered target 304 is placed upon a bottom electrode 303. The target 304 is, for example, $PbTiO_3$, and a high frequency source 305 of electricity is connected across the electrodes 301 and 303 for operation during sputtering. Sputtering gas is introduced through a gas inlet passage 306 and usually consists of 90% argon and 10% oxygen. An additional sputtering gas is introduced through a gas inlet passage 307, and consists of nitrogen containing the vapour of a lead chemical compound. Such a compound may be $Pb(C_2H_5)_4$ or $PbCl_4$, or $Pb_2O(OH)_2$. Because their boiling points are, respectively, 200° C, 105° C and 145° C, they cannot be introduced in their gaseous state at normal temperature. Accordingly, the chemical compound in solid or liquid form is placed as a mass 309 of, for example, $PbCl_4$ in a heating chamber 308. A heater 310 is operated to heat the chamber 308 and to evaporate the compound of the mass 309, which is then introduced into the sputtering chamber by a stream of nitrogen acting as a carrier gas through the gas inlet passage 307. The gas ratio is 85% Ar; 10% O_2; 5% N_2 ($PbCl_4$).

A ferro-electric film of excellent stoichiometric composition is achieved by sputtering when the target is a stoichiometric composition of $PbTiO_3$, the radio frequency power applied is set at 200 W and the substrate temperature is 500° C. The electrical characteristics of such ferro-electric films are such that the data read/write capability is improved to 10^{10}.

The invention may be applied to semi-conductor devices other than that shown in Figure 1. For example, a ferro-electric film may be deposited in accordance with the invention in a structure em-

ploying bi-polar transistors, or on a CMOS structure, or on a bi-polar/CMOS structure. The substrate may also be of other than silicon, for example gallium arsenide.

By the use of the invention, a semi-conductor device having a ferro-electric film of improved stoichiometric composition and crystalline characteristics may be obtained. To achieve this, a constituent element of the film may be doped by ion implantation and thereafter possibly annealed, or sputtering and/or annealing may be performed in an atmosphere containing ozone.

Claims

1. A method of manufacturing a semi-conductor device, comprising the steps of forming a ferro-electric film (110) in the device, and treating the film (110) to improve the stoichiometric composition thereof.

2. A method as claimed in claim 1, wherein the treatment comprises doping the film (110) by ion implantation after formation of the film (110).

3. A method as claimed in claim 2, wherein the doped film (110) is thereafter annealed.

4. A method as claimed in claim 3, wherein the anneal temperature is above 500°C.

5. A method as claimed in claim 3, wherein annealing is performed by rapid thermal anneal.

6. A method as claimed in claim 4 or 5, wherein annealing is performed in an atmosphere containing ozone.

7. A method as claimed in claim 1 wherein the film (110) is formed by sputtering, and the treatment comprises using a sputtering atmosphere containing an element for improving the stoichiometric composition of the film.

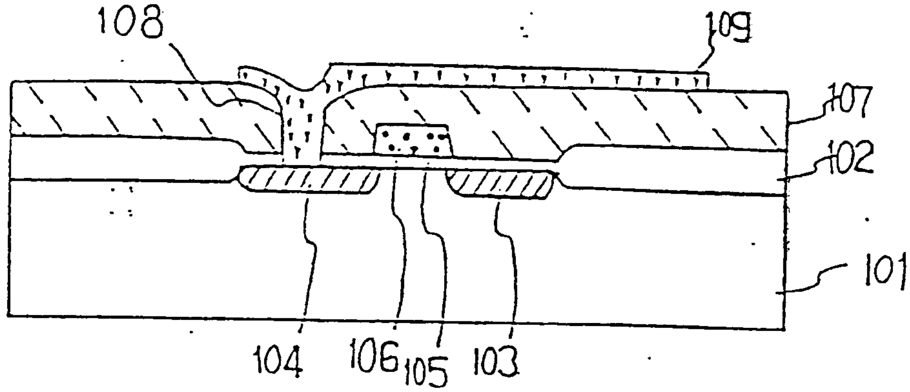
8. A method as claimed in claim 1, wherein the film (110) is formed by sputtering, and the treatment comprises using a sputtering atmosphere containing ozone.

9. A method as claimed in claim 1, wherein the film (110) is formed by sputtering, and the treatment comprises using a sputtering atmosphere containing lead or a lead compound.

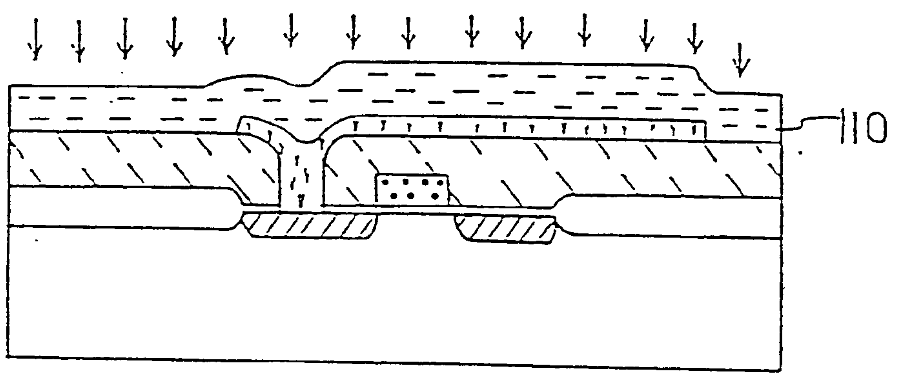
10. A method as claimed in claim 9 wherein the sputtering atmosphere contains at least one of $PbCl_4$, $Pb(C_2H_5)_4$ and $Pb_2O(OH)_2$.

11. A method as claimed in claim 1, wherein the film (110) is formed by sputtering, and the treatment comprises annealing in an atmosphere containing ozone.

12. A method as claimed in any preceding claim, wherein the main component of the ferro-electric film is at least one of $PbTiO_3$, PZT-($PbTiO_3$/$PbZrO_3$) and PLZT(La/$PbTiO_3$/$PbZrO_3$).



F I G 1 (a)



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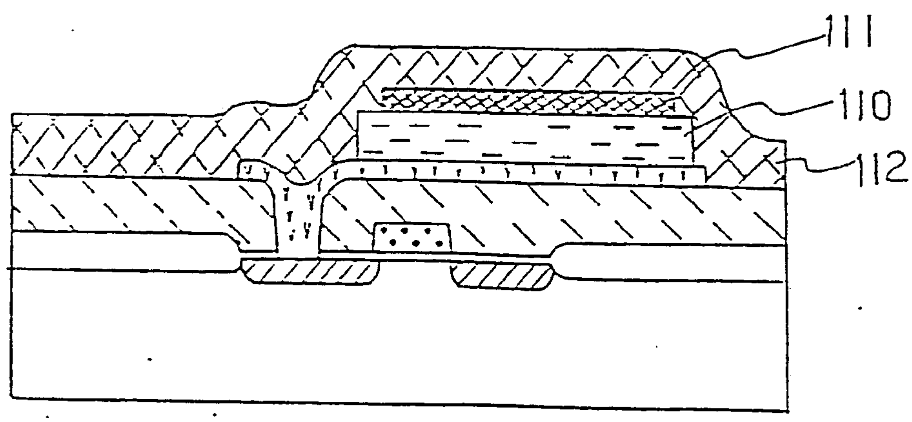
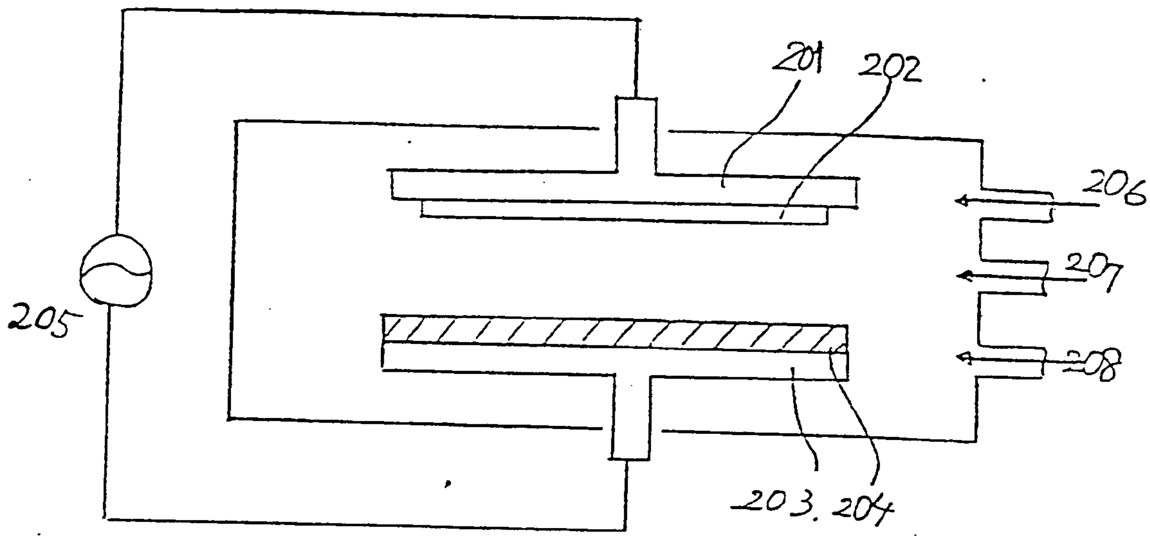
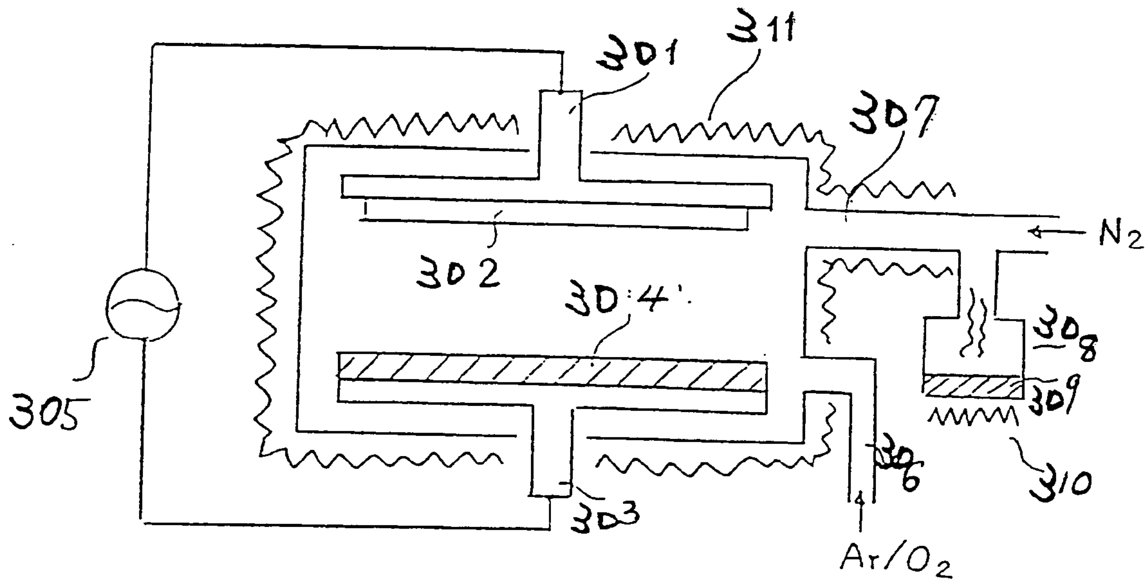


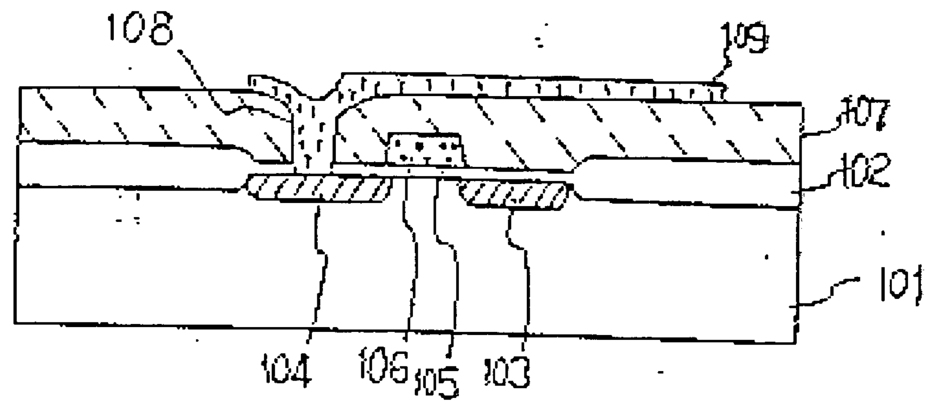
F I G 1 (C)



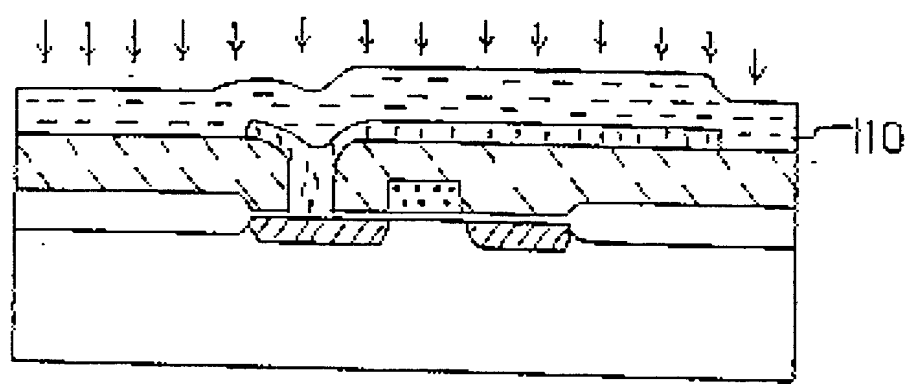
F I G 2



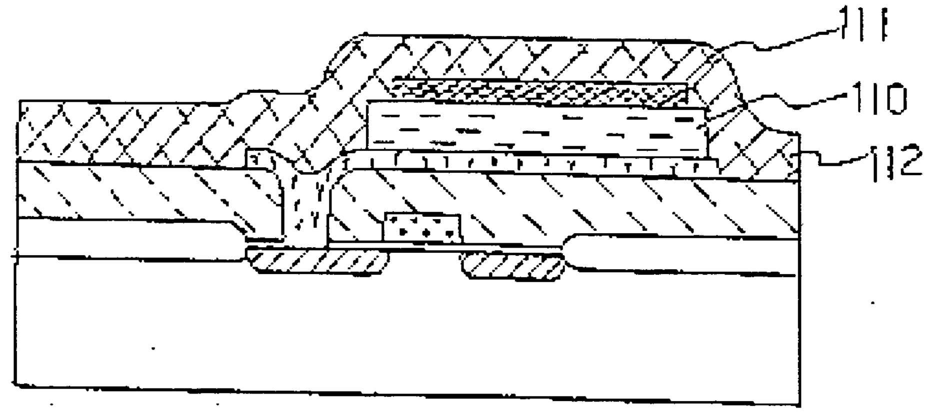
F I G 3



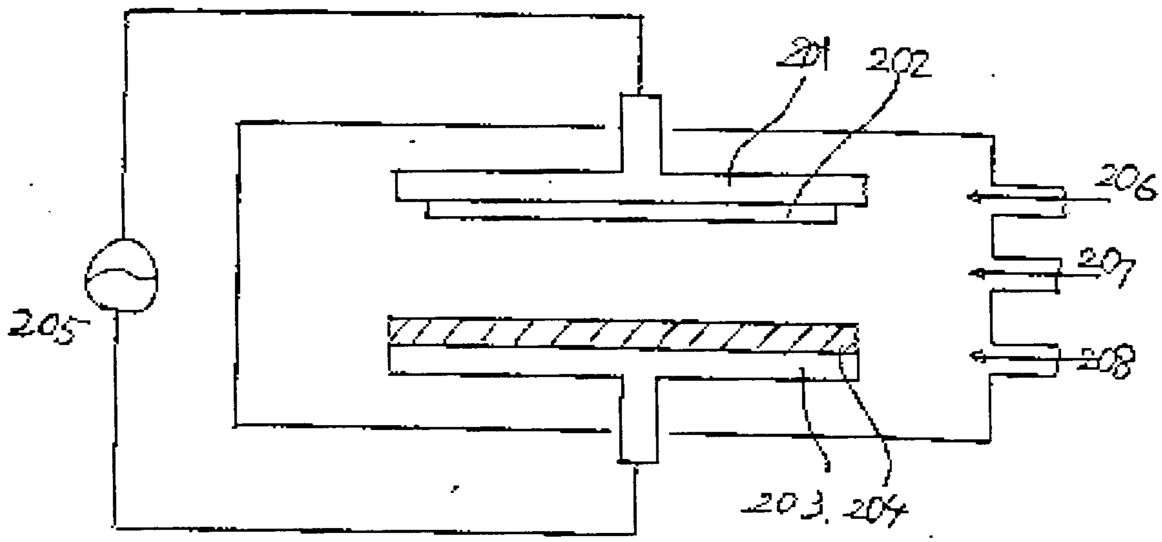
F I G 1 (a)



F I G 1 (b)



F I G 1 (C)



F I G 2

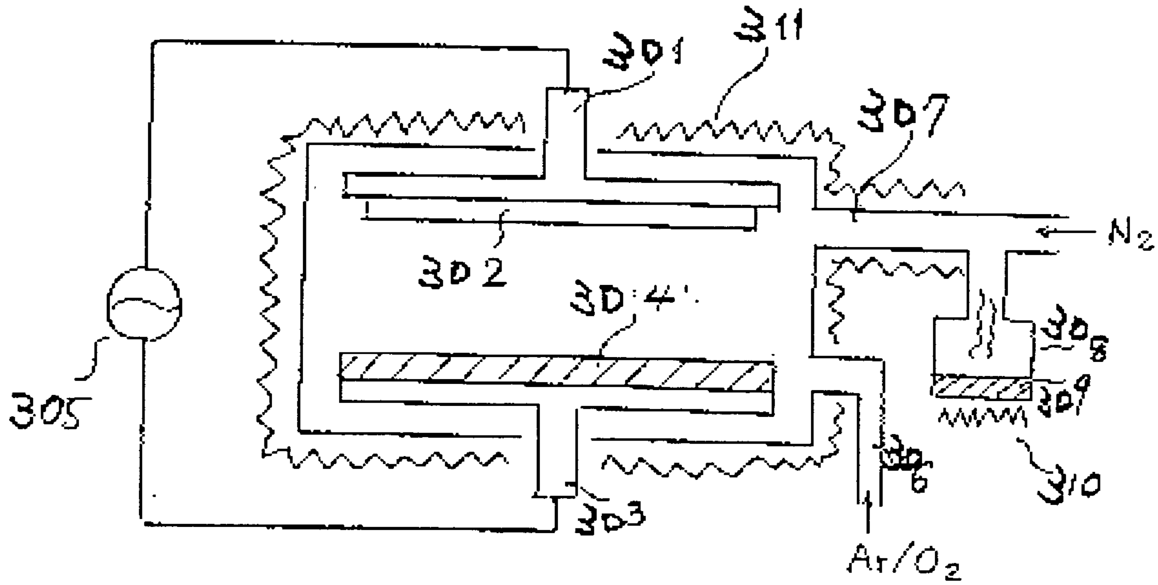


FIG 3